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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A semiconductor bipolar junction device, comprising:

a substrate of semiconductor material having a desired crystalline orientation;

a first semiconductor material extending substantially vertically from said substrate to form a hill having the same crystalline orientation as said substrate;

said first material having a sidewall and an upper surface; and

a ~~second material;~~

~~said~~ second material ~~joined to at least~~ implanted or diffused into a portion of said sidewall and to at least a portion of said upper surface of said first material;

wherein a bipolar junction is formed between said first and second materials.

2. (original): A semiconductor junction device as recited in claim 1, further comprising:

a first electrical contact connected to said first material; and

a second electrical contact connected to said second material.

3. (original): A semiconductor junction device as recited in claim 1, wherein said junction comprises a *pn* junction.

4. (original): A semiconductor junction device as recited in claim 1, wherein said junction comprises an *in* junction.

5. (original): A semiconductor junction device as recited in claim 1, wherein said junction comprises an *pi* junction.

6. (currently amended): A semiconductor bipolar junction device, comprising:

a substrate of semiconductor material having a desired crystalline orientation;

a first semiconductor material extending substantially vertically from said substrate to form a hill having the same crystalline orientation as said substrate;

said first material having at least an upper portion doped with a first impurity ~~comprising a semiconductor material;~~

said first material having a sidewall and an upper surface; and

a ~~second material;~~

~~said~~ second material ~~joined to at least~~ implanted or diffused into a portion of said sidewall and to at least a portion of said upper surface of said first material;

wherein a bipolar junction is formed between said first and second materials.

7. (original): A semiconductor junction device as recited in claim 6, further comprising:

a first electrical contact connected to said first material; and

a second electrical contact connected to said second material.

8. (original): A semiconductor junction device as recited in claim 6, wherein said junction comprises a *pn* junction.

9. (original): A semiconductor junction device as recited in claim 6, wherein said junction comprises an *in* junction.

10. (original): A semiconductor junction device as recited in claim 6, wherein said junction comprises a *pi* junction.

11. (currently amended): A semiconductor bipolar junction device, comprising:

a substrate of semiconductor material having a desired crystalline orientation;

a first material extending substantially vertically from said substrate to form a hill having the same crystalline orientation as said substrate;

said first material having a sidewall and an upper surface; and

wherein an upper portion of said first semiconductor material has been doped with a different type doping than that of the substrate;

a second ~~material;~~

~~said second material comprising a semiconductor material;~~

~~said second~~ material implanted or diffused into ~~joined to~~ at least a portion of said sidewall and to at least a portion of said upper surface of said first material;

wherein a bipolar junction is formed between said first and second materials.

12. (original): A semiconductor junction device as recited in claim 11, further comprising:

a first electrical contact connected to said first material; and

a second electrical contact connected to said second material.

13. (original): A semiconductor junction device as recited in claim 11, wherein said junction comprises a *pn* junction.

14. (original): A semiconductor junction device as recited in claim 11, wherein said junction comprises an *in* junction.

15. (original): A semiconductor junction device as recited in claim 11, wherein said junction comprises a *pi* junction.

16. (currently amended): A semiconductor bipolar junction device, comprising:

a substrate of semiconductor material having a desired crystalline orientation and a first donor impurity type;

a first semiconductor material extending substantially vertically from said substrate to form a hill having the same crystalline orientation as said substrate;

said first material having a sidewall and an upper surface; and

wherein an upper portion of said first semiconductor material is doped with a second donor impurity type;

a second ~~semiconductor material;~~

~~said second~~ material of said first donor impurity type implanted or diffused into ~~joined to~~ at least a portion of said sidewall and to at least a portion of said upper surface of said first material;

wherein a bipolar junction is formed between said first and second materials.

17. (original): A semiconductor junction device as recited in claim 16, further comprising:

a first electrical contact connected to said first material; and

a second electrical contact connected to said second material.

18. (original): A semiconductor junction device as recited in claim 16, wherein said junction comprises a *pn* junction.

19. (original): A semiconductor junction device as recited in claim 16, wherein said junction comprises an *in* junction.

20. (original): A semiconductor junction device as recited in claim 16, wherein said junction comprises a *pi* junction.

21. (currently amended): A semiconductor bipolar junction device, comprising:

a substrate of semiconductor material having a desired crystalline orientation;

a first material extending substantially vertically from said substrate to form a hill of semiconductor material having the same crystalline orientation as said substrate;

~~said first material comprising a doped semiconductor material;~~

wherein an upper portion of said first material is doped with a different type doping than that of the substrate;

said first material having a sidewall and an upper surface; [[and]]

a second ~~material;~~

~~said second material comprising a semiconductor material;~~

~~said second~~ material implanted or diffused into ~~joined to~~ at least a portion of said sidewall and to at least a portion of said upper surface of said first material;

wherein a bipolar junction is formed between said first and second materials;

a doped polysilicon region in contact with one or more sidewalls of said first and/or second material and configured for receiving electrical contacts.

22. (currently amended): A semiconductor junction device as recited in claim 21, further comprising:

a first electrical contact connected to said first material; and

a second electrical contact connected to said second material;

wherein said first and second electrical contacts are connected directly or through said doped polysilicon.

23. (original): A semiconductor junction device as recited in claim 21, wherein said junction comprises a *pn* junction.

24. (currently amended): A semiconductor junction device as recited in claim 21, wherein said junction comprises either an *in* or *pi* junction.

25. (cancelled)

26. (currently amended): A semiconductor bipolar junction device, comprising:

a substrate of semiconductor material having a desired crystalline orientation and a first donor impurity type;

a first material extending substantially vertically from said substrate to form a hill of semiconductor material having the same crystalline orientation as said substrate;

~~said first material comprising a semiconductor material;~~

wherein said first material comprises a portion of said substrate which remains after adjacent portions of substrate material have been etched away;

wherein an upper portion of said first material is doped with a second donor impurity type;

said first material having a sidewall and an upper surface; and

a second material;

said second material comprising a dopant of said first donor impurity type ~~doped semiconductor material~~;

said second material implanted or diffused into ~~joined to at least a~~ an upper portion of a first said sidewall and an adjoining ~~to at least a~~ portion of said upper surface of said first material;

wherein a bipolar junction is formed between said first and second materials.

27. (original): A semiconductor junction device as recited in claim 26, further comprising:

a first electrical contact connected to said first material; and

a second electrical contact connected to said second material.

28. (currently amended): A semiconductor junction device as recited in claim 26, wherein said junction ~~comprises~~ is selected from the group of junction types consisting of *pn, ni, pi* and *pin* junctions ~~junction~~.

Claims 29-30 (Canceled)

31. (currently amended): A semiconductor bipolar junction device, comprising:

a substrate of semiconductor material having a desired crystalline orientation;

a first ~~doped~~ semiconductor material extending substantially vertically from said substrate to form a hill having the same crystalline orientation as said substrate;

wherein said first material comprises a portion of said substrate which remains after adjacent portions of substrate material have been etched away;

wherein an upper portion of said first semiconductor material has been doped;

said first material having a sidewall and an upper surface; [[and]]

a second ~~doped semiconductor material;~~

~~said second~~ material implanted or diffused into ~~joined to at least a~~ an upper portion of a first said sidewall and an adjoining ~~to at least a~~ portion of said upper surface of said first material;

wherein a bipolar junction is formed between said first and second materials;

at least one stopper region formed on the upper portion of said substrate around said hill;

at least one isolation region formed over said at least one stopper region; and

at least two polysilicon regions formed over said isolation regions and in contact with said first and second materials;

said polysilicon regions being configured for receiving contacts for establishing electrical connection to said bipolar junction.

32. (currently amended): A semiconductor junction device as recited in claim 31, further comprising:

a first electrical contact connected to said first material; and

a second electrical contact connected to said second material;

wherein said first and second electrical contacts are connected directly or through said doped polysilicon.

33. (currently amended): A semiconductor junction device as recited in claim 31, wherein said junction ~~comprises~~ is selected from the group of junction types consisting of *pn*, *ni*, *pi* and *pin* junctions ~~junction~~.

34. (withdrawn): A semiconductor junction device, comprising:

a substrate;

a first semiconductor material extending substantially vertically from said substrate;

said first material having a sidewall and an upper surface;

a second semiconductor material;

said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first semiconductor material; and

a third semiconductor material;

said third material joined to at least a portion of said second material;

wherein a first junction is formed between said first and second materials;

wherein a second junction is formed between said second and third materials; and

wherein said first material is electrically isolated from said third material.

35. (withdrawn): A semiconductor junction device as recited in claim 34, further comprising:

a first electrical contact connected to said first material;

a second electrical contact connected to said second material; and

a third electrical contact connected to said third material.

36. (withdrawn): A semiconductor junction device as recited in claim 34, wherein said first junction comprises a *pn* junction.

37. (withdrawn): A semiconductor junction device as recited in claim 34, wherein said first junction comprises an *in* junction.

38. (withdrawn): A semiconductor junction device as recited in claim 34, wherein said first junction comprises a *pi* junction.

39. (withdrawn): A semiconductor junction device as recited in claim 34, wherein said second junction comprises a *pn* junction.

40. (withdrawn): A semiconductor junction device as recited in claim 34, wherein said second junction comprises an *in* junction.

41. (withdrawn): A semiconductor junction device as recited in claim 34, wherein said second junction comprises a *pi* junction.

42. (withdrawn): A semiconductor junction device as recited in claim 34, wherein said first and second junctions are configured as a bipolar transistor.

43. (withdrawn): A semiconductor junction device as recited in claim 42, wherein said bipolar transistor comprises a *npn* transistor.

44. (withdrawn): A semiconductor junction device as recited in claim 42, wherein said bipolar transistor comprises a *pnp* transistor.

45. (withdrawn): A semiconductor junction device as recited in claim 34, wherein said first and second junctions are configured as a *pin* junction device.

46. (withdrawn): A semiconductor junction device as recited in claim 34, wherein said first and second junctions are configured as a *pip* junction device.

47. (withdrawn): A semiconductor junction device, comprising:

a substrate;

a first material extending substantially vertically from said substrate;

said first material comprising a doped semiconductor material;

said first material having a sidewall and an upper surface;

a second material;

said second material comprising a semiconductor material;

said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first material; and

a third material;

said third material comprising a doped semiconductor material;

said third material joined to at least a portion of said second material;

wherein a first junction is formed between said first and second materials;

wherein a second junction is formed between said second and third materials; and

wherein said first material is electrically isolated from said third material.

48. (withdrawn): A semiconductor junction device as recited in claim 47, further comprising:

a first electrical contact connected to said first material;

a second electrical contact connected to said second material; and

a third electrical contact connected to said third material.

49. (withdrawn): A semiconductor junction device as recited in claim 47, wherein said first junction comprises a *pn* junction.

50. (withdrawn): A semiconductor junction device as recited in claim 47, wherein said first junction comprises an *in* junction.

51. (withdrawn): A semiconductor junction device as recited in claim 47, wherein said first junction comprises a *pi* junction.

52. (withdrawn): A semiconductor junction device as recited in claim 47, wherein said second junction comprises a *pn* junction.

53. (withdrawn): A semiconductor junction device as recited in claim 47, wherein said second junction comprises an *in* junction.

54. (withdrawn): A semiconductor junction device as recited in claim 47, wherein said second junction comprises a *pi* junction.

55. (withdrawn): A semiconductor junction device as recited in claim 47, wherein said first and second junctions are configured as a bipolar transistor.

56. (withdrawn): A semiconductor junction device as recited in claim 55, wherein said bipolar transistor comprises a *npn* transistor.

57. (withdrawn): A semiconductor junction device as recited in claim 55, wherein said bipolar transistor comprises a *pnp* transistor.

58. (withdrawn): A semiconductor junction device as recited in claim 47, wherein said first and second junctions are configured as a *pin* junction device.

59. (withdrawn): A semiconductor junction device as recited in claim 47, wherein said first and second junctions are configured as a *pip* junction device.

60. (withdrawn): A semiconductor junction device, comprising:

a substrate;

a first doped semiconductor material extending substantially vertically from said substrate;

said first doped semiconductor material having a sidewall and an upper surface;

a second doped semiconductor material;

said second doped semiconductor material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first doped semiconductor material; and

a third doped semiconductor material;

said third doped semiconductor material joined to at least a portion of said second doped semiconductor material;

wherein a first junction is formed between said first and second materials;

wherein a second junction is formed between said second and third materials; and

wherein said first material is electrically isolated from said third material.

61. (withdrawn): A semiconductor junction device as recited in claim 60, further comprising:

a first electrical contact connected to said first material;
a second electrical contact connected to said second material; and
a third electrical contact connected to said third material.

62. (withdrawn): A semiconductor junction device as recited in claim 60, wherein said first junction comprises a *pn* junction.

63. (withdrawn): A semiconductor junction device as recited in claim 60, wherein said second junction comprises a *pn* junction.

64. (withdrawn): A semiconductor junction device as recited in claim 60, wherein said first and second junctions are configured as a bipolar transistor.

65. (withdrawn): A semiconductor junction device as recited in claim 64, wherein said bipolar transistor comprises a *npn* transistor.

66. (withdrawn): A semiconductor junction device as recited in claim 64, wherein said bipolar transistor comprises a *pnp* transistor.

Claims 67-91 (Canceled)

92. (new): A semiconductor junction device as recited in claim 1, wherein said second material is implanted or diffused into an upper portion of a first sidewall of said first material and an adjoining portion of said upper surface of said first material.

93. (new): A semiconductor junction device as recited in claim 1, further comprising:

a stopper region formed on the top of said substrate around said hill of said first material;

an isolation region deposited or formed over said stopper region; and

at least two polysilicon regions deposited over said isolation region and adapted for receiving electrical contacts.

94. (new): A semiconductor junction device as recited in claim 1, wherein said substrate comprises silicon or silicon-on-insulator.

95. (new): A semiconductor junction device as recited in claim 1, wherein said first material comprises a portion of said substrate which has been doped and about which substrate material has been etched away leaving said hill of said first material.

96. (new): A semiconductor junction device as recited in claim 6, wherein said second material is implanted or diffused into an upper portion of a first sidewall of said first material and an adjoining portion of said upper surface of said first material.

97. (new): A semiconductor junction device as recited in claim 6, further comprising:

a stopper region formed on the top of said substrate around said hill of said first material;

an isolation region deposited or formed over said stopper region; and

at least two polysilicon regions deposited over said isolation region and adapted for receiving electrical contacts.

98. (new): A semiconductor junction device as recited in claim 6, wherein said substrate comprises silicon or silicon-on-insulator.

99. (new): A semiconductor junction device as recited in claim 6, wherein said first material comprises a portion of said substrate which has been doped and about which substrate material has been etched away leaving said hill of said first material.

100. (new): A semiconductor junction device as recited in claim 11, wherein said second material is implanted or diffused into an upper portion of a first sidewall of said first material and an adjoining portion of said upper surface of said first material.

101. (new): A semiconductor junction device as recited in claim 11, further comprising:

a stopper region formed on the top of said substrate around said hill of said first material;

an isolation region deposited or formed over said stopper region; and

at least two polysilicon regions deposited over said isolation region and adapted for receiving electrical contacts.

102. (new): A semiconductor junction device as recited in claim 11, wherein said substrate comprises silicon or silicon-on-insulator.

103. (new): A semiconductor junction device as recited in claim 11, wherein said first material comprises a portion of said substrate which has been doped and about which substrate material has been etched away leaving said hill of said first material.

104. (new): A semiconductor junction device as recited in claim 11:
wherein said substrate is of *p*-type material;
wherein the upper portion of said first material is doped with an *n*-dopant; and
wherein said second material comprises a *p*-type dopant.

105. (new): A semiconductor junction device as recited in claim 16, wherein said second material is implanted or diffused into an upper portion of a first sidewall of said first material and an adjoining portion of said upper surface of said first material.

106. (new): A semiconductor junction device as recited in claim 16, wherein said donor impurity types comprise *p*-dopants and *n*-dopants.

107. (new): A semiconductor junction device as recited in claim 16, further comprising:

a stopper region formed on the top of said substrate around said hill of said first material;

an isolation region deposited or formed over said stopper region; and

at least two polysilicon regions deposited over said isolation region and adapted for receiving electrical contacts.

108. (new): A semiconductor junction device as recited in claim 16, wherein said substrate comprises silicon or silicon-on-insulator.

109. (new): A semiconductor junction device as recited in claim 21, wherein said second material is implanted or diffused into an upper portion of a first sidewall of said first material and an adjoining portion of said upper surface of said first material.

110. (new): A semiconductor junction device as recited in claim 21, wherein said isolation regions comprise oxide.

111. (new): A semiconductor junction device as recited in claim 21, further comprising a stopper region disposed above said substrate.

112. (new): A semiconductor junction device as recited in claim 21, further comprising an isolation region deposited or formed over said substrate region, or over a stopper region disposed above said substrate.

113. (new): A semiconductor junction device as recited in claim 26, further comprising:

a stopper region formed on the top of said substrate around said hill of said first material;

an isolation region deposited or formed over said stopper region; and

at least two polysilicon regions deposited over said isolation region and adapted for receiving electrical contacts.

114. (new): A semiconductor junction device as recited in claim 26, wherein said substrate comprises silicon or silicon-on-insulator.

115. (new): A semiconductor junction device as recited in claim 31, wherein said stoppers comprise *p*-channel stopper regions.

116. (new): A semiconductor junction device as recited in claim 31, wherein said isolation regions comprise oxide.

117. (new): A semiconductor junction device as recited in claim 31, further comprising:

a base contact for the bipolar junction device formed in electrical connection with the top surface of said hill of said first material;

an emitter contact for the bipolar junction device formed in electrical connection through one of said polysilicon regions with said sidewall of said second material; and

a collector contact for the bipolar junction device formed in electrical connection through one of said polysilicon regions with a side surface of said hill of said first material which has not been implanted or diffused with said second material.

118. (new): A semiconductor junction device as recited in claim 117, further comprising passivation regions configured for surrounding one or more of said base, emitter and collector contacts.